**General Information:**

**Name of Course: Digital logic design 2**

**Course Code:** IVB034ANVM

**Semester:** 2nd

**Number of Credits:** 4

**Allotment of Hours per Week:** 1 lectures, 2 practices

**Evaluation: Mid-term** (with grade)

**Prerequisites: Digital logic design 1.**

**Instructors: PETER MEGYERI, master instructor,**

 **ZOLTAN ZIDARICS, department engineer.**

Office: 7624 Hungary, Pécs, Boszorkány u. 2. Office No B233

 E-mail: megyeri@vili.pmmf.hu,

 zamek@vili.pmmf.hu.

 Office Phone: +36 72 503650/23851

**Introduction, Learning Outcomes**

The presentations give an introduction to important digital design principle and methods, the structure and operation of basic combinational, and sequential circuit. Equal emphasis is given to learning new digital devices, like CPLD-s and FPGA-s and to learning how to analyse and synthesize down the operation of different digital circuit and devices.

Upon completion of this course the student should be able to: **interpret,** and **put into practice:**

1. operation and design of different combinational circuits,
2. operation and design of different sequential circuits,
3. structure of multiplexers, comparators, ALUs,
4. structure of storage element, memories, counters, registers, and bus drivers.
5. structure and operation of CPLDs, and FPGAs.

**General Course Description and Main Content:**

Brief Syllabus: This lecture and practical based course aims to give electrical engineering students a solid digital logic design and digital circuit knowledge basis through covering the following topics:

Application of different combinational circuits: multiplexers, comparators, arithmetical and logical units for solving simple control and automation problems.

* Application of different sequential networks: storages, counters, registers, state machines for solving complex control and automation problems.
* Digital logic design methods. Different simplification procedures.
* Electrical characteristics of digital systems. Bus systems. Synchronization and level matching between different systems.

Students learn the basics of digital systems, devices and design methods enabling them to interpret and understand engineering sciences and through solving elementary tasks they deepen their basic theoretical knowledge in the field of digital circuit design. The practical sessions are designed to learn and practice the requirements of digital circuit design.

**Methodology:**

The presentations give an introduction to important digital logic design methods and techniques of exercise solving and the basic structure of different digital circuits. Equal emphasis is given to learning new digital circuits and design principle and to learning how to construct and write down correct digital design solutions.

**Schedule:**

Study period in 15 weeks: February 5 - May 18 (2018)

1. Basics of Combinational networks. Documenting Project. (with Libre-Office), and cognition of digital simulation environment (HADES).
2. Basics of Sequential, and synchronous, and asynchronous networks. Operation and design of Seven-segment display driver.
3. Basic combinational circuits: coder-decoder, and multiplexer. Operation and design of Seven-segment display driver.
4. Comparators, and Arithmetical and logical units. Carry generation. Operation and design of Gray coder.
5. Basic storage element: R-S, J-K storage. Concept of latch and flip-flop. Operation and design of Parity generator.
6. D and T storage. Synchronous and asynchronous operation. Master-slave principle. Operation and design of Half- and full adder.
7. Complex sequential networks: Counters. Operation and design of Counter. **Test1**
8. Complex sequential networks: Registers. Operation and design of State machine.
9. *Spring break*
10. Structure and operation of memories. Operation and design of Synchronous network.
11. Bus systems and bus driver circuits. **Test2.**
12. **Publishing and discussion of Project works.**
13. Classification and features of Programmable Logic Devices. PAL and PLA device. Operation and design of a 4bit Counter.
14. CPLDs and FPGAs. Operation and design of frequency divider.
15. **Administration of Project work.**

Correction period: May 22-24 (2018)

Exam: The subject ends with mid-term grade

**Attendance:**

Attending is required all classes, and will impact the grade (max. 10%). Unexcused absences will adversely affect the grade, and in case of absence from more than 30% of the total number of lesson will be grounds for failing the class. To be in class at the beginning time and stay until the scheduled end of the lesson is required, tardiness of more than 20 minutes will be counted as an absence. In the case of an illness or family emergency, the student must present a valid excuse, such as a doctor's note.

**Evaluation + Grading**

Grading will follow the course structure with the following weight:

1. Class participation, class activity 10 %
2. Project exam 50 %.
3. Tests 40 %
4. Offered exam grade: over 65 % during the study and correction period.

**Grading scale**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Numeric Grade: | 5 | 4 | 3 | 2 | 1 |
| Evaluation in points: | 89%-100% | 77%-88% | 66%-76% | 55%-65% | 0-54% |

**Students with special needs:**

Students with special physical needs and requiring special assistance must first register with the Dean of the Students Office. All reasonable requests to provide an equal learning environment for all students is to be assured.

**Required Reading and other Materials will be equivalent to:**

D. M. Harris and S. L. Harris, ‘Digital Design and Computer Architecture, Morgan Kaufmann, 2007.

Victor P. nelson, h. troy nagle, j. david irwin, bill d. carroll: digital logic circuit analysis & design, prentice hall, 1995.