SUBJECT DETAILS AND SYLLABUS
2020/2021. II. SEMESTER

Subject name	*Digital Logic Design 2.*
Subject code	**IVB034ANVM**
Classes per week: L/P/Lab	**1/0/2**
Number of Credits	**4**
Division/ type	**Electrical Engineering (BSc) / mandatory**
Program	**full time**
Requirement type	**semester rating**
Semester	**2.**
Preliminary requirements	**Digital Logic Design 1.**
Organization name	**Department of Electrical Networks**
Responsible Lecturer(s)	***Zoltan Zidarics, Peter Megyeri***

GOAL OF INSTRUCTION

The course introduces to students the design, testing, and simulation methods of elementary, complex combination and sequential networks of digital technology and their practical use. Shows connections to other areas of expertise and applications.

SUBJECT CONTENT

Brief Syllabus:

Schedule:

Lecture:

1. Combinational networks, synchronous and asynchronous sequential networks.
2. Combinational Networks: Encoders, Decoders, Multiplexers, Arithmetic Units, etc.
3. Elementary Storage Elements: R-S, J-K, D and T flip-flops. Synchronous and Asynchronous operating Storage Elements.
4. More omplex sequential networks.
5. Counters.
6. Shift registers.
7. Electrical characteristics of digital systems: signal level, transfer characteristic, propagation delay, dissipation, fan-out, fan-in).
8. Logic Circuits (TTL, ECL, MOS, CMOS) and comparison between them.
9. Memory types, features, architectures.

10. Presentation of bus systems that are widespread use in practice.
11. Types and operation of registers, bus drives.
12. Grouping and characteristics of programmable logic circuits.
13. Written exam.
14. PAL, PLA type circuits.
15. PLD-, and Complex PLD circuits.

Practice/Labs:

1. Analysis and synthesis of sequential networks. Presentation of the Hades program. Basics of Digital Design. Code Types: BCD, Binary, Gray, etc.
2. Analysis and synthesis of networks containing encoders and decoders. 7-segment display drive.
3. Simulation of networks containing encoders and decoders. Simulation of operation of 7 segment display driver.
4. Design, construction and simulation of parity generator.
5. Arithmetic operation. Design and construction of adder circuits.
6. Practical Exam.
7. Constructing storage circuits using simple gate circuits. Types of storage circuits, characteristics. Debounce. Analysis, synthesis and simulation of sequential networks containing counters.
8. Frequency Division Principles. Design and simulation of frequency dividers.
9. Analysis and synthesis of sequential networks containing registers.
10. Simulation of sequential networks containing registers. Applying memory for making general combination network.
11. Designing synchronous network using storage elements.
12. Design features of bus systems, presentation of their use.
13. Practical Exam.
14. Presentation and control of previously published homework assignments.

EXAMINATION AND EVALUATION SYSTEM

Attendance:

Regarding participation in exercises and lectures, appropriate points of TVSz. are authoritative. According to this, the student cannot obtain the credit point of the subject, if the absence of the relevant classes exceeds 30% of the total number of practices or lectures.

Criterion of Signiture / Semester rating:

Forms of controlling under the semester: written exams, homework. During the semester, students write three exams, two of which are written on practice and one is written on the lecture. The topic of the exams is the material of the practices and lectures given till a given week. The exact time of the exams will be announced in the given classes of the subject. The homework will be released on practice, at the latest until the 10th week. The condition for obtaining the signature is to write the exams and to submit an acceptable homework during the semester.

Exam:

The course ends with a semester rating.

Grading:

The homework and the written exams are evaluated with grades. The weighting used to create the semester rating:
- Homework 50 %.
- Average of written exams 50 %

Grading scale:

Numeric Grade	5	4	3	2	1
Evaluation interval:	90–100%	76–89%	63–75%	51–62%	0–50%

Consultation options:

At the time agreed in advance with the responsible instructor.

LITERATURE

[1.] Victor P. Nelson, H. Troy Nagle, J. David Irwin, Bill D. Carroll: Digital Logic Circuit Analysis and Design, Prentice Hall, ISBN: 0-13-463894-8
[2.] Dr. I. J. Wassell: Digital Electronics, Part I – Combinational and Sequential Logic
[3.] http://american.cs.ucdavis.edu/academic/ecs154a.sum14/postscript/cosc205.pdf
[4.] http://www.panstanford.com/pdf/9789814364591fm.pdf
[5.] Presentations on lectures and practices, and written lecture notes

SCHEDULE

		STUDY PERIOD, STUDY WEEKS														EXAM PERIODK				
2018/2019. II. SEMESTER		1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	1.	2.	3.	4.	5.
Lecture number																					
Partice/Labs number																					
Midterm test															X						
Homework	publishing											X									
	submitting															X					
Signiture/ Semester rating																	X				
Exam																					

07/02/2021.

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Peter Megyeri responsible lecturer