

SUBJECT DETAILS AND SYLLABUS
2021/2022. I. SEMESTER

Subject name	Digital Logic Design 3.
Subject code	IVB036ANVM
Classes per week: L/P/Lab	2/0/2
Number of Credits	5
Division/type	Electrical Engineering (BSc) / mandatory
Program	full time
Requirement type	grade
Semester	5.
Preliminary requirements	Digital Logic Design 2.
Organization name	Department of Electrical Networks
Responsible Lecturer(s)	Peter Megyeri

GOAL OF INSTRUCTION

The course introduces to the students to the theory and practice of various types of programmable logic devices (CPLD, FPGA) and SoC devices, which are widespread used in practice. They will learn across the practical examples how these devices work, how they are designed and how to use them. Besides they will learn how to design those systems, which contain such devices. They are familiar with using of those description languages, which are used to configure these devices (VHDL, Verilog). They get to know the connections to other fields and applications.

SUBJECT CONTENT

Brief Syllabus:

Schedule:

Lecture:

1. Evolution of digital circuits. General purpose logic circuits.
2. Types and grouping of programmable logic circuits.
3. General block diagram and components of programmable logic circuits.
4. Programming and testing of programmable logic circuits.
5. Cell-, and Marco cell based devices: PAL, GAL, HAL, FPLA.
6. Complex, highly integrated devices.
7. Structure, operation, and characteristics of CPLD.
8. Structure, operation, and characteristics of FPGA.

9. Methods of building the logic networks in the programmable circuits.
10. Design and selection aspects of programmable circuits.
11. Testing of logic systems, and circuits: BoundaryScan, JTAG.
12. Structure and operation of elementary BoundaryScan cell.
13. Scanning modes, control signals of test port (TAP).
14. Control of the Boundary Scan Circuits, Test Instructions.

Practice/Labs:

1. The necessity and role of PLDs.
2. Implementation methods of PLDs.
3. Task description techniques.
4. Technical properties of systems.
5. Basics of Hardware Description Languages (Verilog, VHDL).
6. Structure and usage of the Xilinx ISE development system.
7. Implementation of combinational networks.
8. Structure and usage of the simple programmable circuits.
9. Case Study. Implementation of sequential networks.
10. Definition, usage, and significance of the finite state machine (FSM) in digital systems.
11. Structure and usage of CPLDs.
12. Structure, characteristics, and selection aspects of the SoC, SoPC systems.
13. Introduction, application and usage areas of ARM systems.
14. Case Study.

EXAMINATION AND EVALUATION SYSTEM

Attendance:

Regarding participation in exercises and lectures, appropriate points of TVSz. are authoritative. According to this, the student cannot obtain the credit point of the subject, if the absence of the relevant classes exceeds 30% of the total number of practices or lectures.

Criterion of Signiture / Semester rating:

Forms of controlling under the semester: written exam, homework, and project. During the semester, students write an exam, which is written on practice. The topic of the exam is the material of the practices and lectures given till a given week. The exact time of the exam will be announced in the given class of the subject. The topic of the project must be relevant to the subject, and must be agreed in advance with the lecturer of the subject. The homework will be released on practice, at the latest until the 10th week. The condition for obtaining the signature is to write the exam and to submit an acceptable homework, and project during the semester.

Exam:

Written exam, minimum of 51% is required to pass.

Grading:

The written and the practical exams are evaluated with grades. The weighting used to create

the semester rating:

- Homework: 22 %,
- Written exam: 22 %,
- Project: 22 %.
- Written exam in the exam period: 33 %.

Grading scale:

Numeric Grade	5	4	3	2	1
Evaluation interval:	90–100%	76–89%	63–75%	51–62%	0–50%

Consultation options:

At the time agreed in advance with the responsible instructor.

LITERATURE

- [1.] Craig Marven, Gillian Ewers: A simple approach to Digital Signal Processing, Texas Instruments, 1994
- [2.] Robert B. Reese, Mitchell A. Thornton: Introduction to Logic Synthesis using VerilogHDL, Morgan & Claypool 2006,
- [3.] Peter. J. Ashenden: The Designer's Guide to VHDL, Morgan Kaufmann Publisher 2008, 3. Edition,
- [4.] VHDL Reference Manual, Synario Design Automation 1997,
- [5.] Richard E. Haskell & Darrin M. Hanna – „Introduction to Digital Design VHDL”, Digilent Inc-LBEBooks, 2009,
- [6.] Peter Wilson: Design Recipes for FPGAs Using Verilog and VHDL, Newnes is an imprint of Elsevier, 2016,
- [7.] Tertulien Ndjountche: Digital Electronics 3 - Finite-state Machines, Wiley, 2016,
- [8.] Blaine Readler: Verilog by Example A Concise Introduction for FPGA Design,
- [9.] Joseph Cavanagh: Verilog HDL Design Examples, Taylor & Francis Group, 2018,
- [10.] <http://www.xilinx.com/tools/webpack.htm>
- [11.] <http://www.xilinx.com/products/silicon-devices/fpga.html>,
- [12.] <http://www.xilinx.com/support/university.html>,
- [13.] Presentations on lectures and practices, and written lecture notes

SCHEDULE

		STUDY PERIOD, STUDY WEEKS															EXAM PERIODK				
2021/2022. I. SEMESTER		1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	1.	2.	3.	4.	5.
Lecture number																					
Partice/Labs number																					
Midterm test													X								
Homework	publishing								X												
	submitting														X						
Signiture/Semesterrating																	X				
Exam																					

09/10/2021.

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Peter Megyeri responsible lecturer