*Recommended template: “Course Description, Syllabus, Course Requirements”*

# course syllabus and course requirements academic year 2022./2023. semester 1.

| Course title | Project Laboratory 1. |
| --- | --- |
| **Course Code** | **IVB462AN** |
| **Hours/Week: le/pr/lab**  | **0/0/2** |
| **Credits** | **3** |
| **Degree Programme** | **Electrical Engineering BSc** |
| **Study Mode**  | **full-time** |
| **Requirements** | **midterm grade** |
| **Teaching Period** | **fall** |
| **Prerequisites** | **-** |
| **Department(s)****Course Director** | **Department of Automation** |
| **Teaching Staff** | **Kisander Zsolt** |
|  |  |

# course description

*A short description of the course (max. 10 sentences).*

*Neptun: Instruction/Subjects/Subject Details/Basic data/Subject description*

Introductory printed circuit board design.

# syllabus

*Neptun: Instruction/Subjects/Subject Details/Syllabus*

## **goals and objectives**

*Goals, student learning outcome.*

*Neptun: Instruction/Subjects/Subject Details/Syllabus/Goal of Instruction*

Students will learn and practice microelectronic design with CAD systems via guided design projects. Students will have a basic understanding of different design procedures, best practices and pitfalls during a design procedure.

## **course content**

*Neptun: Instruction/Subjects/Subject Details/Syllabus/Subject content*

|  | TOPICS |
| --- | --- |
| LECTURE |  |
| PRACTICE |  |
| laboratory practice | 1. *PCB design suites and their features*
2. *Complete circuit designs, their parts and requirements*
3. *Design cycle, iterative design method*
4. *Agile development*
5. *Technical documentation writing*
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### **DETAILED SYLLABUS AND COURSE SCHEDULE**

### *academic holidays included*

| PRACTICE, LABORATORY PRACTICE |
| --- |
| week | **Topic** | **Compulsory reading; page number****(from … to …)** | **Required tasks (assignments, tests, etc.)** | **Completion date, due date** |
| 1. | Orientation, presenting the requirements |  |  |  |
| 2. | PCB suites I. general features |  |  |  |
| 3. | PCB suites II. overview of a selected suite |  |  |  |
| 4. | Circuit design I. necessary documents |  |  |  |
| 5. | Circuit design II. schematics |  | First design: schematics | next lab |
| 6. | Circuit design III. printed circuit boards (PCB) |  | First design: PCB | next lab |
| 7. | Circuit design IV. manufacturing outputs |  | First design: manufacturing files | next lab |
| 8. | Circuit design V. BOM and written documentation |  | First design: final steps | next lab |
| 9. | Break |  |  |  |
| 10. | Development cycle I. specifications |  | Second design: specification | next lab |
| 11. | Development cycle II. schematics |  | Second design: schematics | next lab |
| 12. | Development cycle III. PCB |  | Second design: PCB | next lab |
| 13. | Agile development |  |  |  |
| 14. | Summary |  |  |  |
| 15. | Grading |  |  |  |

## **assessment and evaluation**

*(Neptun: Instruction/Subjects/Subject Details/Syllabus/Examination and Evaluation System)*

##### **Attendance**

*In accordance with the Code of Studies and Examinations of the University of Pécs, Article 45 (2) and Annex 9. (Article 3) a student may be refused a grade or qualification in the given full-time course if the number of class absences exceeds 30% of the contact hours stipulated in the course description.*

***Method for monitoring attendance*** *(e.g.: attendance sheet / online test/ register, etc.)*

attendance sheet

##### **assessment**

*Cells of the appropriate type of requirement is to be filled out (course-units resulting in mid-term grade or examination). Cells of the other type can be deleted.*

***Course resulting in mid-term grade*** *(PTE TVSz 40§(3))*

***Mid-term assessments, performance evaluation and their ratio in the final grade*** *(The samples in the table to be deleted.)*

| **Type** | **Assessment** | **Ratio in the final grade** |
| --- | --- | --- |
| *First design* |  *max 10 points* | *50%* |
| *Second design* | *max 10 points* | *50%* |
|  |  |  |
|  |  |  |

***Opportunity and procedure for re-takes*** (PTE TVSz 47§(4))

*The specific regulations for improving grades and resitting tests must be read and applied according to the general Code of Studies and Examinations. E.g.: all tests and assessment tasks can be repeated/improved at least once every semester, and the tests and home assignments can be repeated/improved at least once in the first two weeks of the examination period.*

New design project given on the 14th week, with a deadline of the end of the first exam week.

***Grade calculation as a percentage***

*based on the aggregate performance according to the following table*

| **Course grade** | **Performance in %**  |
| --- | --- |
| excellent (5) | 85 % … |
| good (4) | 70 % ... 85 % |
| satisfactory (3) | 55 % ... 70 % |
| pass (2) | 40 % ... 55 % |
| fail (1) | below 40 %  |

The lower limit given at each grade belongs to that grade.

## **Specified literature**

*In order of relevance. (In Neptun ES: Instruction/Subject/Subject details/Syllabus/Literature)*

##### **compulsory reading and availability**

[1.] Linear Circuit Design Handbook, Edited by Hank Zumbahlen, Published by Newnes/Elsevier, 2008, ISBN-978-0-7506-8703-4 (Also published as Basic Linear Design, Analog Devices, 2007, ISBN-0-916550-28-1)

<https://www.analog.com/en/education/education-library/linear-circuit-design-handbook.html> (2022.09.05.)